I. THE CLAIMED INVENTION

As disclosed and claimed, for example by claim 1, the present invention is directed to a method of forming semiconductor memory device capable of electrically writing and erasing data.

The device includes a plurality of cell transistors for storing data, each cell transistor having a floating gate electrode and a control gate electrode, and a plurality of select transistors for controlling and selecting the cell transistors.

A key step of the present invention is that, before the control gate electrodes of the cell transistors are formed, the surface of a substrate directly above channel regions of the select transistors fabricated in the same process as the cell transistors is *exposed*, and gate insulating films of the select transistors are formed on the exposed surface of the substrate. The control gate electrodes of the cell transistors are formed, and gate electrodes of the select transistors are formed on the gate insulating films.

The advantage of the present invention is that the number of fabrication steps is reduced, while still providing the gate oxides and gate structures that are respectively appropriate for the select transistors and the memory cell transistors (see page 9 at line 10 through line 9 of page 10, also page 11 at lines 6-12).

II. THE PRIOR ART REJECTION

The Examiner asserts that US Patent No. 6,265,739 to Yaegashi et al. anticipates the invention, as described by claims 1-4. However, a key feature of the present invention is that before the control gate electrodes of the cell transistors are formed, the select transistor gate oxide is stripped back to the substrate and then rebuilt according to their requirements as differing from the requirements of the memory cell transistor gates.

The Examiner points to Figure 2A-2C of Yaegashi and is understood as alleging that select transistor gate oxide 105 (e.g., under transistor 106) has been stripped and reformed to form a new gate structure. However, it is plain from these figures that no such stripping is performed that would expose the substrate (i.e. p-well 103) under oxide

layer 105, to have the gate oxide then rebuilt according to different conditions. That is, Figure 2A shows a common gate film 105 for the memory cell region and the select transistor region. Figure 2B shows that gate structures 106, 109 are then formed without having stripped back the select transistor gate 105.

The method of the present invention comprises removing the polysilicon of the select transistor regions and the tunnel-gate oxide films at the lower part of the select transistor regions, then forming a new gate oxide film, and forming control gate electrodes using polysilicon.

In contrast, Yaegashi discloses a configuration in which select transistors use a polysilicon which forms the floating gate electrodes of the memory cells. Preferably, this polysilicon is required to be formed with a high resistance to guarantee the hold characteristics of the flash memory. Therefore, without using polysilicon with specific characteristics for the unique function of the select transistors, the select transistors will decline in performance. Additionally, for the gate electrodes of the select transistors, the Yaegashi configuration uses the oxide layer commonly shared with the memory cell floating gate electrodes, which is potentially a source for another degradation of performance.

An advantage of the technique of the present invention is that the number of fabrication steps is reduced, while still providing the gate oxides and gate structures that are respectively appropriate for the select transistors and the memory cell transistors. Yaegashi fails to even mention the problems addressed by the present invention, let alone suggest the solution provided by the technique of the present invention.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "... before forming the control gate electrodes of said cell transistors, exposing a surface of a substrate directly above channel regions of said select transistors fabricated in the same process as the cell transistors ...."

For this reason alone, the claimed invention is fully patentable over the Yaegashi reference. The Examiner introduces the Chen reference to demonstrate that the gate film of the select transistors and the gate film of the periphery transistors can be the same thickness. But Chen contributes nothing to overcome the above-described deficiency of claim 1.

Further, the other prior art of record has been reviewed, but it too, even in combination with Yaegashi or Chen, fails to teach or suggest the claimed invention.

III. Formal matters and Conclusion

Applicant submits that claims 1-6 and 13, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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Frederick E. Cooperrider
Reg. No. 36,769

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254